APPARATUS AND METHOD FOR OUTPUTTING VIDEO DATA

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a display appliance, and more particularly, to an apparatus and method for outputting digital video data in a display appliance.

Description of the Related Art

[0002] Referring to FIG. 1 showing a block diagram of a conventional apparatus for receiving/transmitting digital video data, a transmitter 100 includes a video processor 102 and a D/A converter 104, and a receiver 106 includes an A/D converter 108 and a video processor 110.

[0003] The digital video data outputted from the video processor 102 of the transmitter 100 is converted into an analog video signal by the D/A converter 104. The analog video signal is transmitted to the receiver 106 via a D-sub cable or the like. The A/D converter of the receiver 106 converts the analog video signal received via the D-sub cable into the digital video data. The digital video data is inputted to the digital video processor 110. The video processor 110 converts and outputs the digital video data which is suitable to be displayed. The analog video signal transmitted through the D-sub cable consists of R, G, B, and horizontal and vertical sync signals.

[0004] With the construction as described above, the digital video data is converted into the analog video signal and then the analog video signal is converted into the digital video data, which causes damage to the digital video data.

[0005] In order to solve the above problem, DDWG (Digital Display Working Group) addresses the requirement for a digital interface system transmitting the digital video data in a digital mode. According to DVI (Digital Visual Interface), which is a digital interface system, developed by the DDWG, a transmitting side encodes an input data and various control signals to transmit them via a dedicated connector, while a receiving side decodes the encoded data. The DVI includes TMDS (Transition Minimized Differential Signaling), LVDS (Low Voltage Differential Signaling), GVIF (Gigabit Video Interface) or the like.

[0006] Referring to FIG. 2 showing a block diagram of a transmitter/receiver of TMDS, data inputted to a transmitter 200 includes first digital video data B, second digital video data G, third digital video data R, horizontal and vertical sync signals, first to fourth control data, DE and a clock. A first encoder 202 of the transmitter 200 receives and encodes the first digital video data B, the horizontal and vertical sync signals and the DE, and converts them into serial data to transmit them via a first channel of a TMDS link. A second encoder 204 of the transmitter 200 receives and encodes the second digital video data G, the first and second control data and DE, and converts them into serial data to transmit them via a second channel of the TMDS link. Further, a third encoder 206 of the transmitter 200 receives and encodes the third digital video data R, the third and fourth control data and DE, and converts them into serial data to transmit them via a third channel of the TMDS link. The clock is transmitted via a fourth channel of the TMDS link as is.

[0007] A first encoder 210 of the receiver 208 receives the signals inputted via the first channel of the TMDS link, converts the signals into parallel data, and decodes the signals to output the first digital video data B, the horizontal and vertical sync signals and the DE0. A second decoder 212 receives the signals inputted via the second channel of the TMDS link, coverts the signals into parallel data, and decodes the signals to output the second digital video

data G, the first and second control data and DE1. A third decoder 214 receives the signals inputted via the third channel of the TMDS link, converts the signals into parallel data, and decodes the signals to output the third digital video data R, the third and fourth control data and DE2.

[0008] The output data of the first to third decoders 210 to 214 and the clock received via the fourth channel of the TMDS link are inputted to an inter-channel arranging unit 216. The inter-channel arranging unit 216 arranges various inputted data and the clock to output them in the same format as the inputted format.

[0009] The DVI connector includes a DVI-D connector capable of transmitting/receiving only the digital video data, and a DVI-I connector capable of transmitting/receiving the digital video data and the analog video signal.

[0010] Referring to FIG. 3 showing a view of the pin arrangement of the DVI-D connector, the DVI-D connector includes 12 pins for transmitting the digital video data, 2 pins for transmitting the clock, and 4 pins for DDC.

[0011] Referring to FIG. 4 showing a view of pin arrangement of the DVI-I connector, the DVI-I connector includes 12 pins for transmitting the digital video data, 2 pins for transmitting the clock, 4 pins for DDC, R, G and B pins for transmitting the analog video signal, and pins for transmitting the horizontal and vertical sync signals.

[0012] A conventional apparatus for processing the digital video data inputted in the DVI mode in the display appliance will now be described with reference to FIG. 5.

[0013] The digital video processing apparatus includes a video decoder 300 for receiving and decoding a TV signal to output the decoded signal to a first multiplexer 304, and a component processor 302 for receiving and decoding the DVD signal to output the decoded signal to the first multiplexer 304. The first multiplexer 304 provides a scaler 318 with any one

of outputs of the video decoder 300 and a component processor 302 by control of a microprocessor (not shown).

[0014] A first A/D converter 306 receives the analog RGB signal and converts analog to digital to output the converted signal to a second multiplexer 316. A second A/D converter 308 receives the analog RGB signal inputted via the DVI connector and converts analog to digital to output the converted signal. A DVI decoder 310 decodes the DVI video data inputted through the DVI connector. The data outputted from the DVI decoder 310 is 8:8:8 RGB digital video data. A signal detecting unit 312 detects whether there is a signal in an analog RGB signal input terminal of the DVI connector and a DVI data input terminal, and generates a selection signal according to the detected results. A switching unit 314 selects any one of outputs of the second 2A/D converter 308 and DVI decoder 310 to output the selected output to the second multiplexer 316. The second multiplexer 316 provides the scaler 318 with any one of outputs of the first A/D converter 306 and switching unit 314 by the control of the microprocessor (not shown).

[0015] The scaler 318 scales the digital video data supplied from the first and second multiplexers 304 and 316 to apply the scaled data to the D/A converter 320. The D/A converter 320 converts the digital video data outputted from the scaler 318 into analog video data.

[0016] Some display appliances used commonly do not receive TV signal, DVD signal or the like due to spatial or using restrictions.

[0017] Therefore, it is required to develop a method for outputting digital video data in a display appliance capable of processing only digital video data.

SUMMARY OF THE INVENTION

[0018] Accordingly, the present invention is directed to an apparatus and method for outputting digital video data that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0019] It is an object of the present invention to provide an apparatus and method for outputting digital video data in a display appliance which can receive an analog video signal and converts the signal into DVI video data to output the video data to another display appliance, so that even a display appliance which cannot process the analog video signal can output an image corresponding to the analog video signal.

[0020] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, there is provided a digital video data outputting apparatus in a display appliance, comprising: data converting units for converting various types of analog video signals into digital video data, respectively; an output signal selector for receiving outputs of the data converting units and selecting any one of the received outputs; and an encoding unit for encoding the output of the output signal selector.

[0021] Another aspect of the present invention is to provide a method for outputting digital video data in a display appliance, comprising the steps of: converting video signals inputted to the display appliance into digital video data of a desired format; selecting any one of the digital video data and DVI-encoding the selected data; and outputting the encoded digital video data.

[0022] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by

the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0024] FIG. 1 is a block diagram of a conventional apparatus for receiving/transmitting digital video data;

[0025] FIG. 1 is an exploded perspective view illustrating a laminating frame employing a partial hologram of the present invention;

[0026] FIG. 2 is a block diagram of a conventional transmitter/receiver of TMDS;

[0027] FIG. 3 is a view of the pin arrangement of a DVI-D connector;

[0028] FIG. 4 is a view of the pin arrangement of a DVI-I connector;

[0029] FIG. 5 is a block diagram of a conventional digital audio data processing apparatus;

[0030] FIG. 6 is a block diagram of a digital audio data processing apparatus according to one preferred embodiment of the present invention; and

[0031] FIG. 7 is a detailed block diagram of the output signal selector in FIG. 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0032] Reference will now be made in detail to the preferred embodiment of the present invention, an example of which is illustrated in the accompanying drawings.

[0033] A display appliance according to one preferred embodiment of the present invention receives an analog video signal and converts the signal into DVI video data to output the data to another display appliance, so that a display appliance which cannot process the analog video signal may output an image corresponding to the analog video signal.

[0034] An apparatus for processing digital video data in the display appliance according to one preferred embodiment of the present invention will now be described with reference to FIG. 6.

[0035] The digital video data processing apparatus receives a TV signal which is an analog video signal, a DVD signal, and analog RGB signals, and also receives an analog RGB signal and DVI video data via a DVI-I connector.

[0036] A video decoder 400 receives the TV signal and converts the signal into YIQ or YUV data, of which a luminance component and a color component are divided, and vertical and horizontal sync signals to output YcbCr data. An output of the video decoder 400 is inputted to a first multiplexer 404 and a first CSC (Color Space Converter) 406. The first CSC 406 color coordinate transforms the output of the video decoder 400 to apply it to an output signal selector 426 as first digital RGB data. A component processor 402 converts a DVD signal into the YcbCr data and sync data. The output of the component processor 402 is inputted to the first multiplexer 404 and a second CSC 408. The second CSC 408 color coordinate transforms the output of the component processor 402 to apply it to the output signal selector 426 as second digital RGB data.

[0037] A first A/D converter 410 converts the analog RGB signal inputted via a D-sub connector into third digital RGB data. The third digital RGB data is inputted to a second multiplexer 420 and the output signal selector 426. A second A/C converter 412 converts the analog RGB signal inputted via a DVI-I connector into fourth digital RGB data. The fourth

digital RGB data is inputted to a switching unit 416 and the output signal selector 426. A DVI decoder 414 decodes the DVI video data inputted via the DVI-I connector to output fifth digital RGB data. The fifth digital RGB data is inputted to the switching unit 416 and the output signal selector 426.

[0038] A signal detector 418 connects a pull-up resistor with an analog RGB signal input terminal and a DVI video data input/output terminal of the DVI-I connector. If a signal exists in the analog RGB signal input terminal, the signal detector 418 outputs a signal of '0' level. Meanwhile, if a signal exists in the analog RGB signal input terminal, the signal detector 418 outputs a signal of '1' level. The output of the signal detector 418 is called a first selection signal. The first selection signal is inputted to the switching unit 416 and the output signal selector 426. The switching unit 416 selects one of the outputs of the second A/D converter 412 and DVI decoder 414 according to the first selection signal to apply the selected output to the second multiplexer 420.

[0039] The first multiplexer 404 applies at least one of the outputs of the video decoder 400 and component processor 402 to the scaler 422 by control of the microprocessor 430. The second multiplexer 420 applies at least one of the outputs of the first A/D converter 410 and switching unit 416 to the scaler 422 by control of the microprocessor 430.

[0040] The scaler 422 receives the output of the first multiplexer 404 via the video input terminal, and also receives the output of the second multiplexer 420 via a graphic input terminal. Whether the two input terminals of the scaler 422 are valid is determined by a type of multi mode output of the interested display appliance.

[0041] The scaler 422 processes "amplification", "contraction", "inversion", "keystone", "brightness" and "darkness" for the digital video data inputted under the control of the

microprocessor 430, and applies the results to the D/A converter 424. The D/A converter 424 converts the output of the scaler 422.

[0042] The output signal selector 426 selects any one of the first to fifth digital RGB data by combining the first selection signal, the second selection signal of the microprocessor 430 and a user output enable signal to apply the selected data to the DVI encoder 428. The DVI encoder 428 encodes the digital RGB data outputted from the output signal selector 426, and coverts the encoded digital RGB data into the DVI video data to output the result via the DVI video data input/output terminal.

[0043] Construction and operation of the output signal selector 426 will now be described with reference to FIG. 7.

[0044] The first selection signal is inverted by an inverter I of the output signal selector 426 and then is inputted to a first AND gate A1. The first AND gate A1 takes an AND gate of the first inversed selection signal and the user output enable signal. If a user commands the DVI video data input/output terminal to output the DVI video data in the state that a signal does not exist in the DVI video data input/output terminal, the first AND gate outputs "1", while in other cases, the first AND gate outputs "0". The output of the first AND gate A1 is inputted to the second to sixth AND gates A2 to A6.

[0045] A decoder D decodes the second selection signal provided from the microprocessor 430, and generates outputs corresponding to the second to sixth AND gates A2 to A6, respectively. The outputs are to enable the first to fifth buffers B1 to B5.

[0046] The output terminals of the second to sixth AND gates A2 to A6 are connected to the enable terminals of the first to fifth buffers B1 to B5, respectively. The second to sixth AND gates A2 to A6 receive the outputs of the decoder D one by one, and simultaneously receive the output of the first AND gate A1. If two signals are "1", the interested buffer is enabled.

[0047] The first to fifth buffers B1 to B5 receive the first to N^{th} digital RGB data, and buffers only the digital RGB data supplied when the buffer is enabled.

[0048] With the above description, since the apparatus of the present invention receives the analog video signal and converts the signal into a digital video data, a display appliance which cannot process the analog video signal may output an image corresponding to the analog video signal.

[0049] The foregoing embodiment is merely exemplary and is not to be construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.